IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A device for parallel data processing, wherein the device has at least one matrix of processors arranged in rows and columns, first additional data ports located outside the matrix and second additional data ports located outside the matrix, wherein

the rows are arranged in a stepwise fashion relative to one another,

the columns are arranged in a stepwise fashion relative to one another,

processors have a first processor data port which is connected with one of the first external data ports by means of a first at least straight connection,

processors have a second processor data port which is connected with one of the second external data ports by means of a second at least essentially straight connection, wherein the second at least essentially straight connection is oriented at least essentially orthogonal to the first at least essentially straight connection, and

processors have a first primary processor data port and a first secondary processor data port, wherein the first primary processor data port is formed by the first processor data port and the first primary processor data port of at least one of the processors is also connected with the first secondary processor data port of another processor via the first connection.

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2. (currently amended) A device as claimed in claim 1, wherein the device has a first data buffer for data storage, the first data buffer having first buffer data ports, at least one of which is connected with one of the first external data ports by means of an at least essentially straight third connection that is a continuation of the first connection.

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3. (currently amended) A device as claimed in claim 2, wherein the first data buffer is split up into two physically separated parts of which a first part is positioned close to the first row of

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processors in the processor matrix and a second part is positioned close to the last row of processors in the processor matrix.

4. (currently amended) A device as claimed in claim 1, wherein the device has a second data buffer for data storage, the second data buffer having second buffer data ports, at least one of which is connected with one of the second external data ports by means of a fourth at least essentially straight connection that is a continuation of the second connection.

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5. (currently amended) A device as claimed in claim 4, wherein the second data buffer is split up into two physically separated parts of which a first part is positioned close to the first column of processors in the processor matrix and a second part is positioned close to the last column of processors in the processor matrix.

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6. (canceled).

7. (currently amended) A device as claimed in claim 1, wherein the first primary processor data port and the first secondary processor data port of processors are arranged for receiving data from one of the first external data ports.

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8. (currently amended) A device as claimed in claim 7, wherein the processors are arranged for processing a series of data elements, in which processors are arranged for processing at least one data element from the series of data elements.

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9. (currently amended) A device as claimed in claim 8, wherein processors have a second secondary processor data port, in which the primary processor data port is connected for receiving a data element to be processed from the series of data elements from one of the first external data ports and is connected with the second secondary processor data port of the processor that processes the element preceding the data element in the series of data elements and is also connected with the first secondary processor data port of the processor that processes the data element succeeding the data element in the series of data elements.

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10. (currently amended) A device as claimed in claim 1, wherein processors have a second primary processor data port and a third secondary processor data port, the second primary processor data port being formed by the second processor data port, the second primary processor data port of at least one of the processors also being connected with the third secondary processor data port of another processor via the second connection.

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11. (currently amended) A device as claimed in claim 10, wherein the second primary processor data port and the third secondary processor data port is arranged for receiving data from one of the second external data ports.

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12. (previously presented) A camera system comprising a sensor matrix built up from rows and columns for converting incident electromagnetic radiation into pixel signals, means for converting pixel signals into data and a device comprising processors for parallel data processing as claimed in one of the claims 1.

13. (currently amended) A camera system as claimed in claim 12, wherein the sensor matrix has a color filter matrix and wherein processors are arranged for processing data from a plurality of elements of the sensor matrix, which data contains color information of various colors of the color filter matrix.

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